

# Switching

## SP8M3

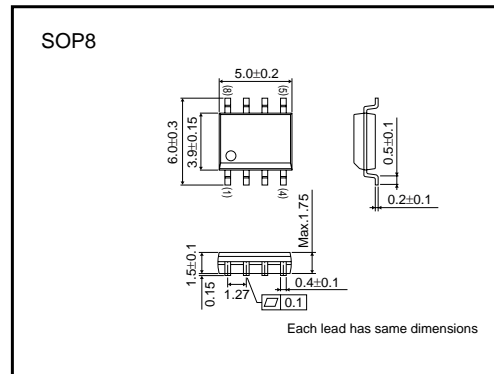
●Features

- 1) Low on-resistance.
- 2) Built-in G-S Protection Diode.
- 3) Small and Surface Mount Package (SOP8).

●Application

Power switching, DC / DC converter.

●External dimensions (Unit : mm)

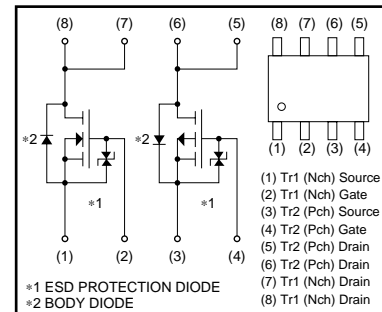


●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits		Unit	
		Nchannel	Pchannel		
Drain-source voltage	V <sub>DSS</sub>	30	-30	V	
Gate-source voltage	V <sub>GSS</sub>	20	-20	V	
Drain current	Continuous	I <sub>D</sub>	±5.0	±4.5	A
	Pulsed	I <sub>DP</sub>	±20	±18	A *1
Source current (Body diode)	Continuous	I <sub>S</sub>	1.6	-1.6	A
	Pulsed	I <sub>SP</sub>	20	-18	A *1
Total power dissipation	P <sub>D</sub>	2		W *2	
Channel temperature	T <sub>ch</sub>	150		°C	
Storage temperature	T <sub>stg</sub>	-55 to +150		°C	

\*1 Pw≤10μs, Duty cycles1%  
\*2 MOUNTED ON A CERAMIC BOARD.

●Equivalent circuit



\*A protection diode is included between the gate and the source terminals to protect the diode against static electricity when the product is in use. Use the protection circuit when the fixed voltages are exceeded.

●Thermal resistance (Ta=25°C)

Parameter	Symbol	Limits	Unit
Channel to ambient	R <sub>th (ch-a)</sub>	62.5	°C / W *

\*MOUNTED ON A CERAMIC BOARD.

## Transistors

## N-ch

## ●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	$I_{GSS}$	–	–	10	$\mu A$	$V_{GS}=20V, V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	–	–	V	$I_D=1mA, V_{GS}=0V$
Zero gate voltage drain current	$I_{DSS}$	–	–	1	$\mu A$	$V_{DS}=30V, V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	1.0	–	2.5	V	$V_{DS}=10V, I_D=1mA$
Static drain-source on-state resistance	$R_{DS(on)}$	–	36	51	m $\Omega$	$I_D=5.0A, V_{GS}=10V$
		–	52	73		$I_D=5.0A, V_{GS}=4.5V$
		–	58	82		$I_D=5.0A, V_{GS}=4V$
Forward transfer admittance	$ Y_{fs} $	3.0	–	–	S	$I_D=5.0A, V_{DS}=10V$
Input capacitance	$C_{iss}$	–	230	–	pF	$V_{DS}=10V$
Output capacitance	$C_{oss}$	–	80	–	pF	$V_{GS}=0V$
Reverse transfer capacitance	$C_{rss}$	–	50	–	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}$	–	6	–	ns	$I_D=2.5A, V_{DD} \approx 15V$
Rise time	$t_r$	–	8	–	ns	$V_{GS}=10V$
Turn-off delay time	$t_{d(off)}$	–	22	–	ns	$R_L=6.0\Omega$
Fall time	$t_f$	–	5	–	ns	$R_G=10\Omega$
Total gate charge	$Q_g$	–	3.9	5.5	nC	$V_{DD} \approx 15V$
Gate-source charge	$Q_{gs}$	–	1.1	–	nC	$V_{GS}=5V$
Gate-drain charge	$Q_{gd}$	–	1.4	–	nC	$I_D=5.0A$

\*Pulsed

## ●Body diode characteristics (Source-Drain Characteristics) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	$V_{SD}$	–	–	1.2	V	$I_S=6.4A, V_{GS}=0V$

\*Pulsed

## Transistors

## P-ch

## ●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I <sub>GSS</sub>	–	–	–10	μA	V <sub>GS</sub> = –20V, V <sub>DS</sub> =0V
Drain-source breakdown voltage	V <sub>(BR) DSS</sub>	–30	–	–	V	I <sub>D</sub> = –1mA, V <sub>GS</sub> =0V
Zero gate voltage drain current	I <sub>DSS</sub>	–	–	–1	μA	V <sub>DS</sub> =–30V, V <sub>GS</sub> =0V
Gate threshold voltage	V <sub>GS (th)</sub>	–1.0	–	–2.5	V	V <sub>DS</sub> = –10V, I <sub>D</sub> = –1mA
Static drain-source on-state resistance	R <sub>DS (on)</sub>	–	40	56	mΩ	I <sub>D</sub> = –4.5A, V <sub>GS</sub> = –10V *
		–	57	80		I <sub>D</sub> = –2.5A, V <sub>GS</sub> = –4.5V *
		–	65	90		I <sub>D</sub> = –2.5A, V <sub>GS</sub> = –4.0V *
Forward transfer admittance	Y <sub>fs</sub>	3.5	–	–	S	I <sub>D</sub> = –2.5A, V <sub>DS</sub> = –10V *
Input capacitance	C <sub>iss</sub>	–	850	–	pF	V <sub>DS</sub> = –10V
Output capacitance	C <sub>oss</sub>	–	190	–	pF	V <sub>GS</sub> =0V
Reverse transfer capacitance	C <sub>rss</sub>	–	120	–	pF	f=1MHz
Turn-on delay time	t <sub>d (on)</sub>	–	10	–	ns	I <sub>D</sub> = –2.5A, V <sub>DD</sub> ≐ –15V *
Rise time	t <sub>r</sub>	–	25	–	ns	V <sub>GS</sub> = –10V *
Turn-off delay time	t <sub>d (off)</sub>	–	60	–	ns	R <sub>L</sub> =6.0Ω *
Fall time	t <sub>f</sub>	–	25	–	ns	R <sub>G</sub> =10Ω *
Total gate charge	Q <sub>g</sub>	–	8.5	–	nC	V <sub>DD</sub> ≐ –15V *
Gate-source charge	Q <sub>gs</sub>	–	2.5	–	nC	V <sub>GS</sub> = –5V *
Gate-drain charge	Q <sub>gd</sub>	–	3.0	–	nC	I <sub>D</sub> = –4.5A *

\*Pulsed

## ●Body diode characteristics (Source-Drain Characteristics) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V <sub>SD</sub>	–	–	–1.2	V	I <sub>S</sub> = –1.6A, V <sub>GS</sub> =0V *

\*Pulsed

Transistors

N-ch

●Electrical characteristic curves

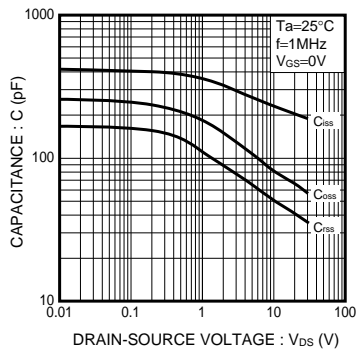


Fig.1 Typical Capacitance vs. Drain-Source Voltage

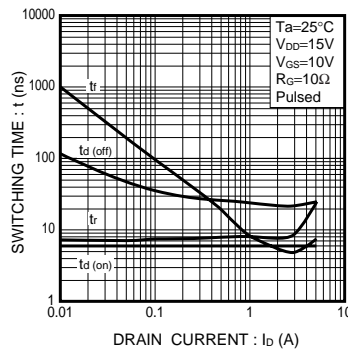


Fig.2 Switching Characteristics

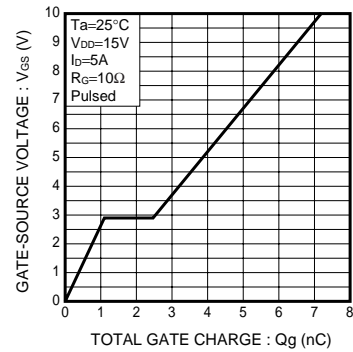


Fig.3 Dynamic Input Characteristics

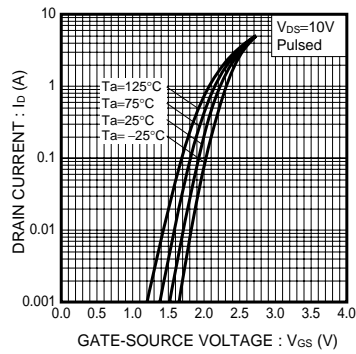


Fig.4 Typical Transfer Characteristics

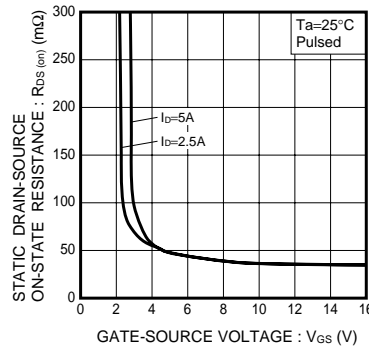


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

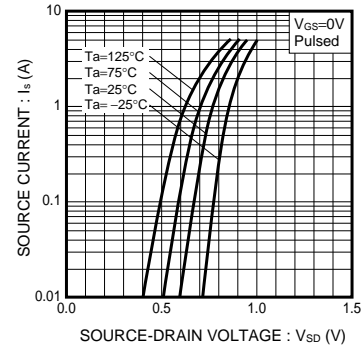


Fig.6 Source Current vs. Source-Drain Voltage

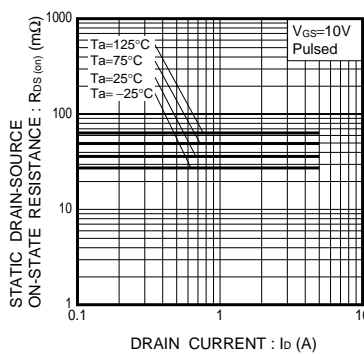


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (I)

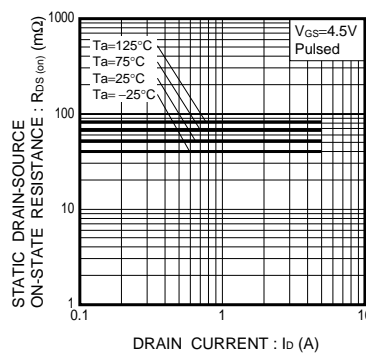


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (II)

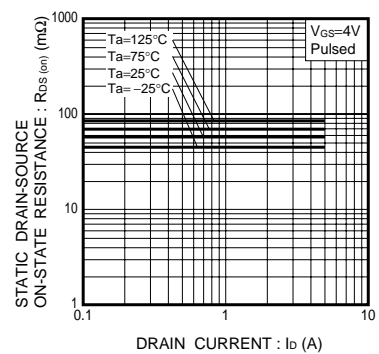


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (III)

Transistors

P-ch

●Electrical characteristic curves

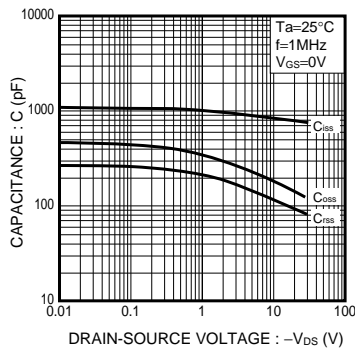


Fig.1 Typical Capacitance vs. Drain-Source Voltage

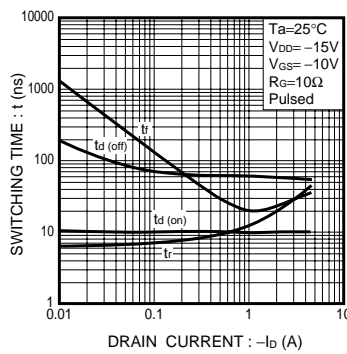


Fig.2 Switching Characteristics

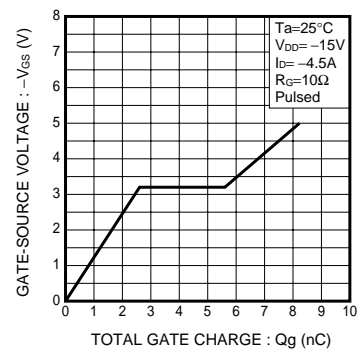


Fig.3 Dynamic Input Characteristics

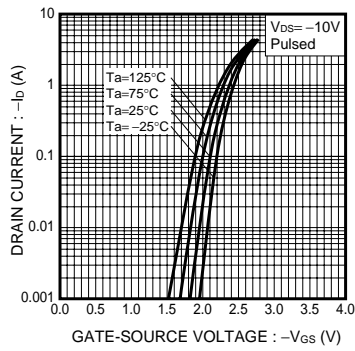


Fig.4 Typical Transfer Characteristics

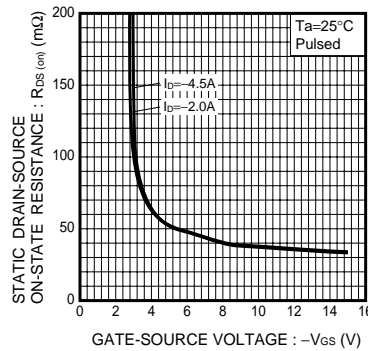


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

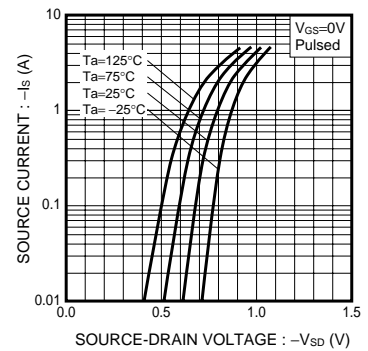


Fig.6 Source Current vs. Source-Drain Voltage

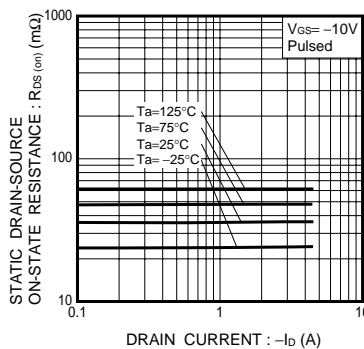


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (I)

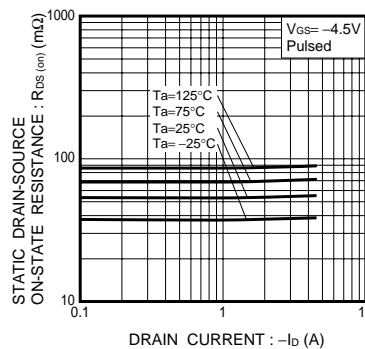


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (II)

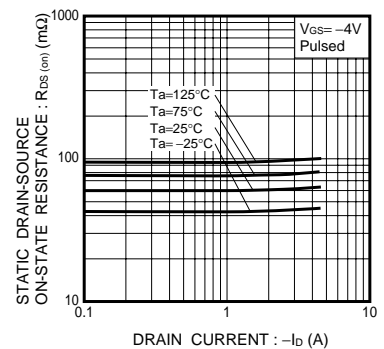


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (III)

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